"Recent Developments and Future Trends in System-in-Package (SiP) and Embedded Passives Technologies"

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Cambridge
Outline

• Introduction
• Portable product trends
• Embedded passives technologies
• System-in-Package technologies
• Design methodologies
  • The ADEPT-SiP project
• Past, present & future growth
• Summary and conclusions
Introduction

Dr. David Pedder (M.A. Cantab. Ph.D.)
Technology Manager, Consultant - Microtechnology, TWI Ltd, Cambridge, UK

Interests: advanced packaging & interconnection, flip chip bonding, embedded passives, process technology, materials..

Background: Plessey Research, GPS, Visiting Professor, CTO - Intarsia Corp., NAC on Devices & Materials, IMAPS UK, ITIC, EU expert reviewer

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Microtechnology

• Materials joining @ <1mm scale
  – Welding & bonding
  – Device packaging
  – Surface mount & soldering
  – Environmental impact
  – Precision reliability
  – Prototyping and validation
Portable product trends

• Manufacturing competence shift
  OEMs (Original Equipment Manufacturers) →
  EMS (Electronic Manufacturing Services)
  & ODMs (Original Design Manufacturers)
• Supply Chain Management key to productivity
• Business processes spanning multiple sites
• Manufacturing shift to China
• Environmental legislation impact
Portable product trends

• Cell phone functionality growing
  – imaging, web access, email, Bluetooth ..

• Wireless networking, automotive entertainment
Portable product trends

- Silicon device size slowing
- Silicon feature size reduction slowing
- Portable & consumer product ramps accelerate
  - release to peak production - 3 to 6 months
  - production end + 18 months or less
- LCD & plasma displays displacing CRT
- New MEMS applications emerging
- System-in-Package usage growing
Discrete passive components

On a typical PCB, discrete passives comprise:

- 91% of components
- 29% of solder joints
- 41% of board area
- ~ 1 trillion passives surface-mounted per annum
- ~ 0.5 cents purchase + 1.3 cents “conversion”
- Passives numbers growing
Surface Mount component issues

- Yield
- Discrete values: E-series
- Solder joint reliability
- Performance & pad parasitics
- Placement constraints
Embedded Passives

- Embedded Passives benefits
  - Improved performance
  - Reduced size & weight (2 to 10 fold)
  - Higher functional density
  - Reduced mounted component count
  - Reduced costs per function
  - Reduced wiring demand
  - Greater SMT throughput
  - Improved reliability & EMC emissions
  - Continuous component values
  - Lead-free technology
  - High added value & IPR protection
Embedded Passive Options

- **On-Chip**
  - performance & costs constraints
  - emerging technology for SoC integration

- **Thin-film**
  - highest resolution, performance & passives density
  - growing manufacturing base

- **LTCC**
  - mature basic technology
  - improving dimensional control

- **PCB**
  - Emerging capabilities
  - Attractive cost-performance benefits
On-chip passives

- **Standard CMOS, BiCMOS, bipolar processes**
  - $L_s$: $Q$ limited by Al metallisation, substrate losses
  - $C_s$: values limited by low $\varepsilon_r$ materials
  - $R_s$: accuracy, TCR limited by polysilicon properties

- **Emerging CMOS, BiCMOS, SoI processes**
  - $L_s$: copper BEOL metallisation, thick dielectric layers
  - $C_s$: specific capacitor layers
  - $R_s$: specific resistor layers
Thin-film passives

• Substrates
  – Silicon or glass: wafer or LAP format
• Ls
  – thick Al or Cu metallisation
• Cs
  – MIM capacitors to 1nF/mm²
  – Pit capacitors > 25nF/mm²
• Rs
  – TaN, NiCr resistors
  – @ ~ 100Ω/square
Thin-film applications

- **IPDs**
  - Matching, biasing, filters
- **RF modules**
  - GSM, Bluetooth, HIPERLAN
LTCC passives

- Substrates
  - Multilayer glass-ceramic
- Ls
  - thick-film Ag alloy metallisation
- Cs
  - glass-ceramic
  - ferroelectric
- Rs
  - Thick-film resistors
  - 10 to 10MΩ/square
LTCC applications

RF modules
- Bluetooth, TxRx
PCB passives

• Substrates
  – FR4, HDI: panel format
• Ls
  – Cu metallisation
• Cs
  – laminate ~ 0.30nF/cm²
  – PTF ~ 3nF/cm²
  – CTF ~ 150nF/cm²
• Rs
  – NiP, Pt alloy, PTF, CTF
PCB applications

- SiP modules
  - Portable products
- Board level
  - Digital, mixed signal
Technology comparison

<table>
<thead>
<tr>
<th>Applications:</th>
<th>RF</th>
<th>RF/Digital</th>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology:</td>
<td>Organic</td>
<td>LTCC</td>
<td>Thin-film</td>
</tr>
<tr>
<td>Key Attributes:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low K</td>
<td>best</td>
<td>good</td>
<td>best</td>
</tr>
<tr>
<td>Low loss</td>
<td>fair</td>
<td>best</td>
<td>best</td>
</tr>
<tr>
<td>High cap. density</td>
<td>poor</td>
<td>fair</td>
<td>good</td>
</tr>
<tr>
<td>High Q inductors</td>
<td>best</td>
<td>good</td>
<td>best</td>
</tr>
<tr>
<td>Reliability</td>
<td>good</td>
<td>best</td>
<td>good</td>
</tr>
<tr>
<td>Accurate patterning</td>
<td>good</td>
<td>good</td>
<td>best</td>
</tr>
<tr>
<td>2-sided attachment</td>
<td>best</td>
<td>best</td>
<td>poor</td>
</tr>
<tr>
<td>Vias</td>
<td>good</td>
<td>good</td>
<td>best</td>
</tr>
<tr>
<td>Cost</td>
<td>best</td>
<td>good</td>
<td>poor</td>
</tr>
<tr>
<td>Attach actives</td>
<td>best</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>Multi-patterns</td>
<td>best</td>
<td>good</td>
<td>best</td>
</tr>
<tr>
<td>Termination flexibility</td>
<td>best</td>
<td>tbd</td>
<td>fair</td>
</tr>
<tr>
<td>Primary Difficulty:</td>
<td>materials</td>
<td>shrinkage</td>
<td>cost</td>
</tr>
<tr>
<td>Primary Advantage</td>
<td>cost</td>
<td>mature</td>
<td>Functional density, performance</td>
</tr>
<tr>
<td>Optimum size:</td>
<td>&gt;100mm²</td>
<td>50mm²</td>
<td>&lt;25mm²</td>
</tr>
</tbody>
</table>

- Source: Korony, Galvani & Heisand, IMAPS Workshop - Passive Integration, Ogunquit, June 2002
SiP benefits

- **System-on-Chip (SOC)**
  - Low cost in volume
  - High NRE costs
  - Performance compromises

- **System-in-Package (SiP)**
  - Multiple active & passive die
  - Standard package outline
  - Stacked Die, modules, MCMs, 3D
  - Flexibility
  - Faster time-to-market
  - Lower NRE
  - Higher performance
### ITRS Roadmap for SiP

**System-in-Package (SiP) applications**

<table>
<thead>
<tr>
<th>YEAR OF PRODUCTION</th>
<th>2004</th>
<th>2007</th>
<th>2010</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology ½ pitch (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
</tr>
<tr>
<td>Terminals, RF</td>
<td>150</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Body size, (L x W) (mm)</td>
<td>50</td>
<td>52</td>
<td>52</td>
<td>52</td>
</tr>
<tr>
<td>Terminal pitch, BGA (mm)</td>
<td>1.00</td>
<td>0.80</td>
<td>0.50</td>
<td>0.50</td>
</tr>
<tr>
<td>Terminal pitch, leadless (mm)</td>
<td>0.50</td>
<td>0.50</td>
<td>0.50</td>
<td>0.40</td>
</tr>
<tr>
<td>No. Stacked die</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Total SiP die</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>Discrete passives chip size</td>
<td>0201</td>
<td>01005</td>
<td>01005</td>
<td>01005</td>
</tr>
<tr>
<td>Embedded passives</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>MSL level</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Maximum reflow temperature (°C)</td>
<td>260</td>
<td>260</td>
<td>260</td>
<td>260</td>
</tr>
</tbody>
</table>

*ITRS 2003

*Design and modelling identified as a key barrier*
Design methodologies

• SMT design
  – component values
    • limited to E-Series
    • limited no. of footprints
  – engineering change
    • value changes possible after pcb manufacture
    • minimal impact on NPI cycle time
Design methodologies

- Embedded passives substrate design
  - component values
    - quasi-continous, semi-infinite geometries
  - engineering change
    - requires redesign, mask changes, repeat pcb manufacture
- Right-first-time design essential
  - requires accurate passive and active device models
  - requires rigorous design simulation, design yield simulation, component generation, layout, DRCs, LVS ...
  - Rigorous pwb lot parametric acceptance testing advised
  - Manufacture & test of individual functional blocks advised
  - Manufacture & test of design variants advised
Design route development

- Well-defined process architecture
- Stable process & known capabilities
- Produce component characterisation boards
- RFOW measurements
- S-parameter extraction
- Model generation
- Design kit integration

Source: IMEC, Intarsia/Dow
Component models

- Integrated passive components
  - interconnect
    - microstrip line, CPW line, discontinuities
  - inductors
    - planar, square, spiral, stacked
  - capacitors
    - MIM, inter-digitated, 3D
  - resistors
    - linear, serpentine

- Assembly structures
  - die attach pad, wire bond, flip chip bond & pads
  - module to next-level interconnect

Source: IMEC, Intarsia/Dow
Design route application

- design specification
- schematic capture - hierarchical
- simulation & optimisation
- component generation
- circuit layout
- re-simulation
- design tolerance & yield
- design for test, reliability....
- mask layout
- verification - DRC, LVS
- design documentation

World Centre for Materials Joining Technology
Design example - filter

- Operational Frequency 0.9GHz
  - Insertion Loss < 0.7dB
  - Return Loss > 15.0dB
- Out of Band Response
  - Attenuation > 30dB@ 1.8GHz
  - Attenuation > 30dB@ 2.7GHz

Source: Intarsia/Dow
Design partitioning

- Partitioning key to size, cost, performance
- Opportunities for chip-package co-design
- Many partitioning options
  - SoC, SiP
  - pcb, LTCC, thin film, on-chip passives
  - hierarchical design helpful
  - easy interface transfer helpful
- Performance & cost-per-function Figures-of-Merit
Functional Level FOMs

- Performance FOMs
- Function specific: e.g. 2GHz VCO design

3ML Al BEOL
5ML Cu BEOL (M4//M5 + shield)
3ML Al + add-on 4 um Cu module
WLP-1: 16um BCB / 5 um Cu (Si_{float})
WLP-2: 16um BCB / 10 um Cu
MCM-D: 16um BCB / 10 um Cu / AF45

\[
FOM_{VCO} = 10 \cdot \log \left( \frac{\omega}{\omega_m} \right)^2 \frac{1}{P_{N_{\text{ref}}}} \cdot I_i \cdot Vdd
\]

Source: IMEC
Functional Level FOMs

• Cost per function FOM
  \[ C_{pf} = C_{pa} \cdot A_c \cdot E_l^{-1} \cdot Y_d^{-1} \cdot Y_m^{-1} \]

  where
  \( C_{pf} \) = cost per function
  \( C_{pa} \) = cost per unit area
  \( A_c \) = total components area
  \( E_l \) = layout efficiency
  \( Y_d \) = design yield
  \( Y_m \) = manufacturing yield
Design for test

• At design phase
  • identification of probable pads on nets
  • Simulation of net impedance - active devices removed
  • simulation at process limits & with anticipated defects
  • identification of detectable defects

• At pcb manufacture
  – individual layers pre-lamination
    • resistor test & trim
  – after board manufacture
    • PCM test and parametric lot acceptance
    • net probe measurements and comparison with simulation
    • pwb acceptance/rejection
Thin film SiP module test

Substrate Design-for-test

LAP manufacture

LAP panel PCM acceptance test

Substrate test

KGD procurement → KGD assembly

Module packaging

Module RF functional test

Source: Intarsia/Dow
ADEPT-SiP project

Advanced Design, Partitioning and Test for System-in-Package Electronics (ADEPT-SiP)

- DTI Technology Programme
  - Design, Modelling & Simulation
- 9 partners
- 36 months project
- **Objective:** To develop and demonstrate a right-first-time design and supply chain management methodology for novel System-in-Package electronic product functions
Partners & Roles

- **TWI** - assembly, packaging, reliability, environment
- **Filtronic** - SiP & GaAs design, SiP build, end-user
- **Zarlink** - SiP & silicon design, SiP build, end-user
- **Zuken** - design tools development, supply chain
- **QuantumCAD** - substrate & package design
- **Wurth Elektronik** - PCB design & manufacture
- **Flomerics** - thermal & EMC modelling, supply chain
- **Leeds** - design, measurement, models, design kits
- **AWR** – design kits, design route integration
ADEPT-SiP Architecture

ADEPT-SiP module

encapsulation

active devices

embedded passives

HDI substrate

motherboard
## System-in-Package (SiP) Unit Shipments Mu*

<table>
<thead>
<tr>
<th>Product</th>
<th>2005</th>
<th>2006</th>
<th>Leading suppliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacked die in package</td>
<td>1,200</td>
<td>1,500</td>
<td>ASE, Amkor, Stats ChipPAC, Spansion, Sharp, Intel</td>
</tr>
<tr>
<td>Stacked Package on Package</td>
<td>55</td>
<td>80</td>
<td>Amkor, Stats ChipPAC, ASE ..</td>
</tr>
<tr>
<td>Wafer or Die Level Module</td>
<td>7</td>
<td>10</td>
<td>Matrix, Infineon</td>
</tr>
<tr>
<td>Mobile phone front-end modules</td>
<td>1,083</td>
<td>1,300</td>
<td>RFMD, Skyworks, Freescale, Philips, Renesas, Amkor, ASE</td>
</tr>
<tr>
<td>Mobile phone transceiver and radio modules</td>
<td>15</td>
<td>30</td>
<td>Murata, Skyworks, Renesas, Freescale, Amkor, ASE</td>
</tr>
<tr>
<td>Bluetooth and WLAN</td>
<td>122</td>
<td>150</td>
<td>CSR, Alps, Mitsumi, Sony, Philips, Infineon, Murata, Gennum</td>
</tr>
<tr>
<td>Graphics/CPU MCM</td>
<td>25</td>
<td>28</td>
<td>Amkor, ASE, SPIL, IBM, Fujitsu, Renesas</td>
</tr>
<tr>
<td>Leadframe modules</td>
<td>345</td>
<td>410</td>
<td>Philips, ST, TI, Freescale, Toshiba, NEC, Infineon</td>
</tr>
<tr>
<td>Power modules</td>
<td>25</td>
<td>35</td>
<td>Toshiba, Renesas, PowerOne, IR, Fairchild, OnSemi</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2,877</td>
<td>3,543</td>
<td>-</td>
</tr>
</tbody>
</table>

*INEMI 2007
Future developments

- **Applications Focus**
  - High clock speed, high frequency, size critical

- **Technology focus**
  - LTCC
    - intermediate size RF modules
  - Thin-film
    - active plus passive IPDs
    - smaller SiP modules
  - PCB embedded
    - Board and larger SiP modules
    - Much HDI synergy
Future developments

• Timescales
  – Gated by
    • technology development & characterisation
    • design tools development
    • applications development
    • industry infrastructure development
  – Date for >25% of all multilayer PWBs using one or more embedded layers
    • 2012
Summary

• Portable products technology driver
• Embedded passives and SiP
  • Major cost-performance benefits
  • An important differentiator
  • The next step beyond SMT
• Design methodologies key
Thank you for your attention

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