The “Conductive Lithographic Film (CLF)” circuit fabrication process is a method of forming electronic circuit interconnect and components on flexible substrates via the offset lithographic printing process.
Overview

- Conductive Lithographic Films (CLF) – A short history 1995 onwards
- The power problem
- Integrated printed electronic systems via the offset lithographic printing process?
CLF - A short history..

- Harrison, Billett & Billingsley began investigations into a circuit fabrication techniques for reduced environmental impact in 1996
- The process described involved the deposition of silver-loaded conductive ink via offset lithographic printing
- It was envisaged that if successful this could vastly reduce the environmental impact associated with the production of standard PCBs
- Offset had speed and material advantages over the alternative screen printing
Offset Lithography

- A standard technique for manufacturing books
- Quite different to so called "Photo-Lithography"
- Relies on dissimilar wetting functions on the surface of an un-embossed printing plate
Offset Lithography Properties

- High resolution (line widths < 25 microns).
- Very high speed.
- 6000 - 10000 Impressions per hour on a Heidleberg GTO46.
- Very low cost (dominated by substrate).
Conductive Lithographic Films (CLF)

- Purpose developed lithographic inks containing electronic materials
- Electrical conductors can be printed on flexible substrates
- Low sheet resistance (< 0.15 ohms per square)
- Dielectric, resistive, ferrite & semi conducting films, forming composite circuit structures
CLF demonstrator circuits

- A microcontroller driven thermometer
- Circuit interconnect, resistors, capacitors and switch actuator all printed by offset lithography
- Uses a glazed paper circuit substrate
Further developments...

- Two further lithographic circuit fabrication strategies based on plating seeding have been devised and implemented.

- One process uses an ink containing micro-particulate silver, which can be electro-less and then electro-plated to form solid copper interconnect.

- The other (3rd-generation) process avoids the use of precious metals entirely, and uses a standard metal oxide powder which is chemically reduced to form a plating seeding layer.
Printed Humidity Sensors

- Capacitive type humidity sensor formed using parallel plate theory
- Change in capacitance relies on change in permittivity of substrate with ingress of moisture

![Graph showing the relationship between capacitance (pF) and relative humidity (%).]
Printed Strain Sensors

- Structures designed to exploit piezoresistive effect of ink film
- Single track and solid block planar configurations evaluated
- Printed of six alternative substrates:
  - GlossArt, PolyArt
  - Teslin, Kapton
  - Melinex, Mylar C
- Structures fabricated and evaluated using silver and graphite based ink formulations
Strain – Resistance Results

- Responses generated from single track configurations printed with silver loaded conductive ink
- Typical plots of fractional change in resistance due to strain for each substrate
- Structures exhibit sensitivity, linearity and hysteresis comparable to structures formed via screen printing methods
Printed Semiconductor Films

- Extrinsic Semiconductor Particulate (CuO)
- Semiconductor Ink Films Overprint Interdigitated CLF Conductor Structure
- Finished Sensors Exhibit Temperature/Resistance Profile Consistent With Extrinsic Semiconductor With Band-Gap 1.1eV
Printed Conductor Structure

Copper (II) Oxide
Printed electrode film (3-5 μm)
Substrate (200μm thick)
Temperature Response

![Graph showing temperature response]
Lithographically Printed Voltaic Cells

• What?
• Investigate the fabrication of voltaic cells (electric cells & batteries) by offset lithography

• Why?
• Costly additional processes and materials required for power

• IeMRC-funded 12 month feasibility study ran from October 2005 to September 2006 with industrial partners:
Initial work

- Zinc – Carbon ‘Leclanche’ chemistry chosen

- Initial cells fabricated to prove an electrochemical potential could be produced using CLF deposited inks

- Two inks developed for anode and cathode electrode fabrication

Zinc and Carbon:
- Particulate
- Resin
- Solvent
- Anti-oxidant

Both inks displayed shear thinning and viscosity values around 7-9 Pas at a shear rate of 400 sec$^{-1}$
Cell structures

- Silver current collectors
- MnO₂ paste
- Printed on non porous substrate material
Cell internal resistance

- **Ra** - the resistance of the electrochemical path including the electrolyte and the separator.
- **Rm** - is the resistance of the metallic path through the cell including the terminals, electrodes and interconnect.
- **Cb** - the capacitance of the parallel plates which form the electrodes of the cell.
- **Ri** - is the non-linear contact resistance between electrode and the electrolyte.
Early cell tests and peak currents

Two substrate materials:
- PolyArt
- Melinex

Three different thickness of cathodic paste:
- 500 μm
- 250 μm
- 125 μm

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<th>Substrate</th>
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<th>Approximate peak current (mA)</th>
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Cell discharge curves

- PolyArt deposited electrodes
Battery demonstrator

Demonstrator printed on PolyArt substrate material

Includes four cells, producing a potential of 6 – 6.5V

Incorporates printed switch pads

Surface mount LEDs and resistors attached with conductive adhesive
Lithographically Printed Integrated Electronics

- Research into the development and fabrication of integrated electronic circuits by the offset lithographic printing process
- 18 month IeMRC-funded project began October 2006. Due to finish March 2008
- Improving printed batteries performance and research applications with:
  * ‘Intelligent paper’
  * RFID
  * Displays
  * Biosensors
- Industrial Partners:
CLF printed electroluminescent displays

- Interdigitated electrode structures formed using standard CLF conductive ink
- Electroluminescent ink deposited on electrode structure
CLF printed electroluminescent displays

- Interdigitated electrode structures formed using standard CLF conductive ink (100 microns T & G), generating a field strength of $2 \times 10^4$ V/cm at 200 V AC
CLF displays

- CLF printed thermochromic display
- Heating elements printed using resistive ink
- Thermochromic ink deposited above
- **Progress**
  - Voltaic cells developed with improved performance
  - Initial work on integrated systems carried out
  - Other chemistries investigated
  - Electrochemical Impedance Spectroscopy (EIS) analysis of cells
Darren Southee
spent eight years working in the electronics industry in service, production and design roles. He designed the TD201 Digital Storage Adapter for THANDAR Electronics Ltd (1987) and the TA320 Logic Analyser for TTi Ltd (1992). His academic career has included roles at Bournemouth University – researching non-invasive blood sugar measurement, Bradford University (UAE) and the University of Lincoln. He is currently Course Director for the undergraduate programme in Industrial Design & Technology at Brunel University and a member of the Cleaner Electronics Research Group. He has been an investigator on grants awarded by the EU, EPSRC and PARK.
Darren’s primary research over the past four years has been the development of printed power sources and he has been PI on two IeMRC (EPSRC) grants in this area. Recent research outputs include two patents and four journal publications in printed electronics. He is a member of the IET and a Fellow of the Higher Education Academy.