“The Role of Flip Chip Bonding in Advanced Packaging”

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“The Role of Flip Chip Bonding in Advanced Packaging”

- Flip Chip Definitions
- Flip Chip Technologies
- Flip Chip Properties
- Flip Chip Applications
- Flip Chip – The Future
- Summary & Conclusions
Flip Chip Definitions *

- **Flip**
  “A mixture of beer & spirits sweetened with sugar and heated with a hot iron”

- **Chip**
  “A counter used in games of chance”

- **Bond**
  “in a state of serfdom or slavery”

or ..... 

Flip Chip Definitions *

- Flip Chip Bonding - The connection of a device, bond pads face down, onto a substrate with a matching array of bond pads.
Flip chip bonding history

• 1960
  - IBM develops Solid Logic Technology

• 1964
  - Totta and Miller develop the C4 process
  - C4 = Controlled Collapse Chip Connection
Flip chip bonding evolution

- 3 bonds/chip 1964 Cu ball transistor
- 10-30 bonds/chip 1970 C4 SSIC
- 120 bonds/chip 1980 C4 LSI
- 354 bonds/chip 1985 C4 VLSI
- 2100 bonds/chip 2000 C4 SoC
Flip chip bonding advantages

• Very high interconnection density
  Area array and peripheral bonds possible
  Fine pitch (50\,\mu m) connections possible

• Improved high frequency/speed performance
  Short/repeatable connection length
  Reduced electrical parasitics

• Minimal component footprint
  True chip scale package
Flip chip bonding technologies

- Solder flip chip
- Adhesive flip chip
- Solid phase flip chip
Solder flip chip bonding

- **Common uses**
  - Flip chip on board (FCOB)
  - Flip chip in package (FCIP)
  - System in package (SiP)
  - Hybrid modules

- **Solder advantages**
  - Self aligning (<1 μm)
**Solder flip chip bonding**

**Bumping**
- Controlled dewetting
- CrCuAu wettable metal
- 95Pb5Sn solder

**Bonding**
- Limited wettable areas
- Surface tension controlled alignment
  stand-off

Device

- As deposited
- Reflowed
- CrCu/CuSn

Substrate

- Oxide
- AlSi
- Passivation
**Solder flip chip bond design**

- Balance of surface tension & gravitational forces
- Conservation of volume allows joint design
- Surface tension dominates
- Double truncated sphere approximation
- Sets solder uniformity requirements, mixed bond design
Solder flip chip bond design

- Solder volume uniformity requirements

\[ \Theta = 0^\circ \quad \Theta = 180^\circ \quad \text{Perimeter volume} \]

- Solder volume uniformity requirements
Solder flip chip bond design

As deposited
- 125 µm
- 70 µm
- 6.9 µm
- 43 µm

Reflowed
- 33.5 µm
- 23.8 µm

Bonded
- 20.8 µm
- 3.0 µm

- Matched 18 & 70 µm bond design
Solder flip chip bond alignment

- Solder vernier structure
- Alignment $< 2\mu m$ vernier resolution
Solder bumping

- Wafer level processing
- Under bump metallisation (UBM)
  - Ohmic contact
  - Adhesion/barrier between the pad and the bump
  - Wettable surface
- Common UBM deposition techniques
  - Plating
  - Evaporation
  - Sputtering
- Typical UBMs
  - Ni/Au
  - Cr/CrCu/Cu/Au
  - NiV/Cu
  - TiW
Solder bumping

- Typical solder alloys
  - High melting point Lead/Tin (95/5) solder
  - Eutectic Tin/Lead (63/37) solder
  - Lead-free solder: Tin/Copper/Silver etc
  - Eutectic Gold/Tin (80/20) solder

- Common solder deposition techniques
  - Evaporation
  - Plating
  - Stencil printing
  - Laser dispense
  - Mould transfer
**Solder bumping underfill**

- Required for flip chip on board (FCOB) reliability
- Underfill process
  - underfill dispense
  - underfill cure

![Diagram showing solder bumping underfill process](image)

- Dispense needle
- Underfill drawn under die by capillary action

- Flip Chip Integrated Circuit
- Laminate Printed Circuit Board
Solder bumping reliability

- Low cycle thermal fatigue

Factors:
- Cycle amplitude
- Chip size
- CTE mismatch
- Solder alloy
- Bond geometry
- Use of underfill
Adhesive flip chip bonding

- Common uses
  - Chip on glass (COG)
  - Chip on flex (COF)

- Adhesive advantages
  - Fine pitch (50µm)
  - Low temperature process
  - No separate underfill required (Anisotropic Conductive Adhesive)
  - Lead-free
Adhesive flip chip wafer bumping

- Wafer level processing
- Common bump deposition techniques
  
  Gold stud bumps formed with a gold ball bonder
  Electroless plated nickel bumps/thin immersion gold
  Electrolytic plated gold bumps, typically on a TiW UBM
  Polymer bumps (selectively placed conducting adhesive)
Adhesive flip chip bonding

Heated pick-up tool

Integrated Circuit Die

Substrate

Anisotropic Conductive Film (conductive particles in a non-conductive adhesive)
Adhesive flip chip bonding
Solid phase flip chip bonding

- Common uses
  - Flip chip on board (FCOB)
  - Flip chip in package (FCIP)
  - System in package (SIP)
  - Hybrid modules

- Die pads require bumping
  - Gold stud bumps
  - Electroplated gold bumps
Solid phase bonding processes

Heat, compression

Thermocompression

Heat, compression, ultrasonic vibration

Thermosonic

Hesse & Knipps
Solid phase bump coining

Individual/gang coining
## Solder flip chip bond properties

<table>
<thead>
<tr>
<th>Bonding Parameter</th>
<th>Wire Bond</th>
<th>TAB</th>
<th>Flip Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material(s)</td>
<td>Al</td>
<td>Au</td>
<td>Cu</td>
</tr>
<tr>
<td>Melting temperature, °C</td>
<td>660</td>
<td>1064</td>
<td>1084</td>
</tr>
<tr>
<td>Typical bond geometry</td>
<td>25µm diameter x 2.5mm length</td>
<td>25x100µm tape x 2.5mm length</td>
<td>100µm diameter x 80µm height</td>
</tr>
<tr>
<td>Typical pitch, µm</td>
<td>100µm perimeter</td>
<td>200µm perimeter</td>
<td>200µm area</td>
</tr>
<tr>
<td>Bond strength, grams</td>
<td>6</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Bond resistance, m.ohms</td>
<td>142</td>
<td>122</td>
<td>17</td>
</tr>
<tr>
<td>Interbond capacitance, pF</td>
<td>0.025</td>
<td>0.025</td>
<td>0.006</td>
</tr>
<tr>
<td>Bond inductance, nH</td>
<td>2.6</td>
<td>2.6</td>
<td>2.1</td>
</tr>
<tr>
<td>Thermal resistance °C/mW per bond</td>
<td>80</td>
<td>52</td>
<td>8</td>
</tr>
<tr>
<td>No. of I/Os per chip</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4mm chip size</td>
<td>160</td>
<td>160</td>
<td>80</td>
</tr>
<tr>
<td>8mm chip size</td>
<td>320</td>
<td>320</td>
<td>160</td>
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</tbody>
</table>
Flip chip industry infrastructure

- Wafer bumping
  Over 20 companies established
- Flip chip substrates
  ~20 companies established
- Flip chip equipment
  Over 20 manufacturers established
- Flip chip assembly services
  Over 30 subcontractors
Flip chip applications

- Silicon devices
  - Discretes
  - RFICs - SiGe
  - ASICs, Microprocessors & System-on-Chip
- GaAs devices
- Integrated Passive Devices (IPDs)
- System-in-Package (SiPs)
- 3D Integration
- Photonics Assemblies
  - device and substrate alignment
  - spatial light modulator
- Sensors
  - Uncooled, cooled IR sensors
  - HDD readers
Flip chip discretes

Source: National Semiconductor.
Flip chip on lead

SOT23

MLP

Source: Carsem.
Flip chip RFIC

Bluetooth Radio Module

RF IC: 46 flip chip bonds at 200µm pitch

Thin film integrated passive substrate

40 BGA balls at 0.80mm pitch

Source: Intarsia.
Flip chip CPU IC

Pentium II chip: 2100 flip chip bonds at 250 µm pitch

BGA substrate

570 BGA balls at 1.27 mm pitch

Mini-cartridge substrate

240 way connector

Source: Intel
Flip chip GaAs

Source: GMMT
Flip chip IPDs

Source: CMD

Source: Telephus
Flip chip SiPs

Source: Intarsia.

Source: STMicroelectronics
Flip chip SiP utilisation

SiP technologies - die level

Source: eKTN
Flip chip 3D integration

Why 3-D?
“More than MOORE”

<table>
<thead>
<tr>
<th>EMC3D Estimations</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Size Reduction</td>
<td></td>
</tr>
<tr>
<td>15%</td>
<td></td>
</tr>
<tr>
<td>Power/signal</td>
<td></td>
</tr>
<tr>
<td>30%</td>
<td></td>
</tr>
<tr>
<td>Improvement</td>
<td></td>
</tr>
<tr>
<td>40%</td>
<td></td>
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<tr>
<td>Cost Increase</td>
<td></td>
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<tr>
<td>5%</td>
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3.8mm X 2.9mm

SOC solution:
- Reduced system size
- Increased performance
- Increased device cost

3D stack:
- Reduced system size
- Short interconnects
- Reduced packaging cost

Source: iNEMI, IMEC
Flip chip 3D integration

Source: iNEMI, Renesas
Flip chip 3D integration

16Gb memory (8 x 2Gb) 560μm

50μm thick Chip

TSV

Laser drilled via

Micro bump

Source: iNEMI, Samsung
Flip chip photonics devices

Source: GMMT
Flip chip IR sensor devices

Source: Irisys
Flip chip hard disc sensor devices

Source: Seagate
Flip Chip Trends

- Much wider uptake
  2% to 10% all devices
  IPDs & high I/O devices
- Growth of infrastructure
- New technologies
  Cu pillar bumping
- Lower cost processes
- Finer pitch
  Chip-to-chip bonding
- Improved reliability

Source: TechSearch International, Inc.

Source: ChipWorks
Flip Chip Futures

- Flip chip usage will continue to grow
- Drivers
  - High I/O applications
  - Where size is critical
  - High frequency/speed applications
  - IPDs, SiPs, 3D integration
Thank you for your attention

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