IeMRC Innovative electronics Manufacturing Research Centre

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Design for X

Research Issues:

- Test strategies
- Collaborative design
- Rapid prototyping
- Partitioning
- Multiphysics tools
- High frequency
- DFAssembly
- DfDisassembly
- Power management
- DfRecycling
- Thermal management
- Optics
- Reliability
- DfManufacture
- Low volume DfManufacture
- Tests for reliability
- Lead free

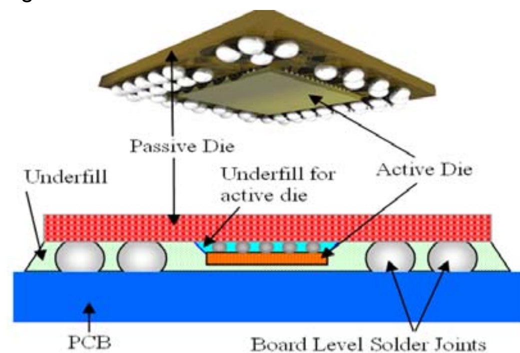
Participating investigators:

Dr David Selviah	UCL	Dr Andrew West	Loughborough University
Prof D Harrison	Brunel University	Prof. Rachel Thomson	Loughborough University
Prof Marc Desmulliez	Heriot Watt University	Prof. Andrew Richardson	Lancaster University
Dr Changhai Wang	Heriot Watt University	Dr Alton Horsfall	University of Newcastle
Prof. Mark Johnson	University of Nottingham	Dr John Lanham	UWE
Prof. Chris Bailey	Greenwich University	Dr Linda Newnes	University of Bath

Introduction

The complexity of next generation systems, coupled with their sensitivity to conflicting factors (cost, processing, packaging, testability, reliability and environmental impact), is creating demands on design and manufacturing. Solving these conflicts requires a transition from performance-driven design, to design where manufacturability, sustainability and manufacturing effectiveness (e.g. agility) are driving forces of an integrated process. At present much of the design within an organisation and through its supply chain is disjointed. At each stage in the process from chip through to PCB then system, designers optimise their own segment; oblivious to the impacts they have on other stages. A solution may draw on combinations of mathematical modelling, rules for resolving conflicts, structured partitioning and hierarchical decomposition, which must link to many design tools to provide the supportive environment needed to produce complex designs.

Exemplar: Design for Manufacture of System-in-Package (SiP) technologies:
SiP is any combination of semiconductors plus optionally other components such as passives, MEMS, and optical components assembled into a single package. Positioned to enable More-Than-Moore SiP has a number of major challenges in terms of design as it requires co-design between chip, PCB, and packaging and to be able to capture the failure mechanisms that can occur in these complex designs. An IeMRC project in collaboration with industry has started to address this international challenge.



Lancaster and Greenwich Universities have been developing Design-for-Manufacture methodologies and models that predict impact of manufacturing processes on solder joint life for particular SiP structures.

Vision

The vision of this theme is to provide underpinning research into design methodologies that will enable the UK electronics industry to retain and enhance its competitive edge in high added value and low-volume sectors.

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Strategy

DfX technologies will be central to the continued success of the electronics manufacturing sector in the UK. Directed through its industrial steering group, calls and review processes, the IeMRC is responding to this challenge by supporting DfX activities which bring together leading UK researchers with industry to address the key design challenges facing UK industry today and in the future.

Objectives

- Deliver a portfolio of research into design methods that will support existing strengths and underpin the development of future markets for the UK electronics sector.
- Support other IeMRC themes to develop new solutions for electronics in challenging environments including research in materials, processes, packaging and test.

Collaboration

Research groups supporting this theme have benefitted from opportunities to collaborate with industry and other research groups within the IeMRC. Industry has given extensive support in the form of equipment, technology samples and characterisation/access to facilities. Academic groups have collaborated on a range of issues including health monitoring for MEMs devices, reliability testing and through-life cost estimating. Collaborations outside the IeMRC have included TSB-funded projects, EU-funded projects and EPSRC projects (responsive mode and Grand Challenge).

Review and future research priorities

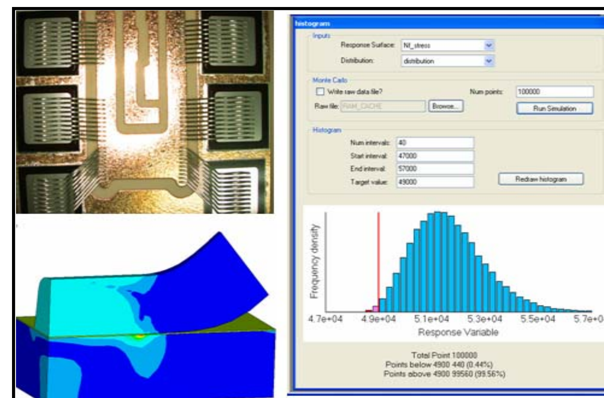
Projects supported under the DfX theme have dealt with a number of emerging topics in electronics manufacturing including: design methodologies for system in package (SiP); design methods for complex, low volume electronics; Physics of Failure (PoF) models for power electronic modules; prognostics and health management; through-life cost estimating within defence systems. Selected highlights include:

1. Multi-Physics models that integrate prediction of electric fields, temperature, cure kinetics, and stress have been developed to aid in the development of novel micro-engineered microwave oven in the FAMOBS project. Results from this project have provided the material for a future FP7 proposal.

2. A novel design methodology for design for manufacture for SiP has had an impact on industrial partners NXP Semiconductors (optimising solder joint design) and SELEX (helping it qualify the product for application).

Exemplar: Physics-of-Failure (PoF) Models and Risk-Based Design for Reliability of Power Electronics Modules

Working closely with UK industry the IeMRC Power Electronics flagship project has developed a methodology to generate PoF models that predict failure mechanisms in power models. These together with reduced order models for stress predictions, and monte-carlo based risk analysis is developing a six-sigma driven approach to predictive reliability.



Greenwich and Nottingham Universities have been developing PoF models and Risk-Based software for Power Module Designers.

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3. PoF based lifetime models for SnAg solder joints have been developed in the Power Electronics Flagship. Comparisons between predicted failures and experimental results show good agreement. The PoF work within this flagship feeds into the TSB-funded MPM project which is developing a PoF-based design tool for power electronic modules.

4. A model for the evolution of the microstructure in SnAgCu solders with increasing exposure has been developed and differences which have been observed experimentally in respect of the size and morphology of the Cu6Sn5 and Cu3Sn intermetallic compounds can be explained by it application.

Further DfX work will continue to provide design and simulation support to the other IeMRC theme areas. Future research will develop new, improved, and integrated DfX tools to address the emerging design needs of the UK electronics manufacturing industry and its supply chain. This will include:

- Continued development of DfX for next generation heterogeneous systems and SiP technologies. Process models, design rules, and test technologies that support co-design between packaging and chip designers (<65nm) and board designers (signal rates >10Gb/s) to offer low cost solutions.
- Development and validation of modelling & simulation tools (i.e. High fidelity and reduced order multi-physics/scale and stochastic models) for electronics manufacturing processes to help support ***DfManufacturabilty***, ***DfPackaging***, ***DfReliability***, ***DfTestability, DfYield,*** *and* ***DfEnvironment, etc.***
- Interfacing with best practice and developments taking place internationally. In particular at establishments such as IZM Fraunhofer (Germany), IMEC (Belgium) and CALCE (USA).